**INTRODUCTION TO MODELSIM AND GATE LEVEL MODELING**

**Lab no# 01**

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CSE-308L Digital Systems Design lab

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“On my honor, as student of University of Engineering and Technology, I have neither given nor received unauthorized assistance on this academic work.”

Student Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_

Submitted to:

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**Gate Level Modeling**

**Task 01:** Implement a buffer at the gate level.

**Design Code:**

module buffer(in,out);

input in;

output out;

buf b(out,in);

endmodule

**Test Bench:**

module testbench1();

reg in;

wire out;

buffer tb(in,out);

initial

begin

$display("in, Out");

in=0;

#10 $display("%b,%b",in,out);

in=1;

#10 $display("%b,%b",in,out);

in=0;

#10 $display("%b,%b",in,out);

in=1;

#10 $display("%b,%b",in,out);

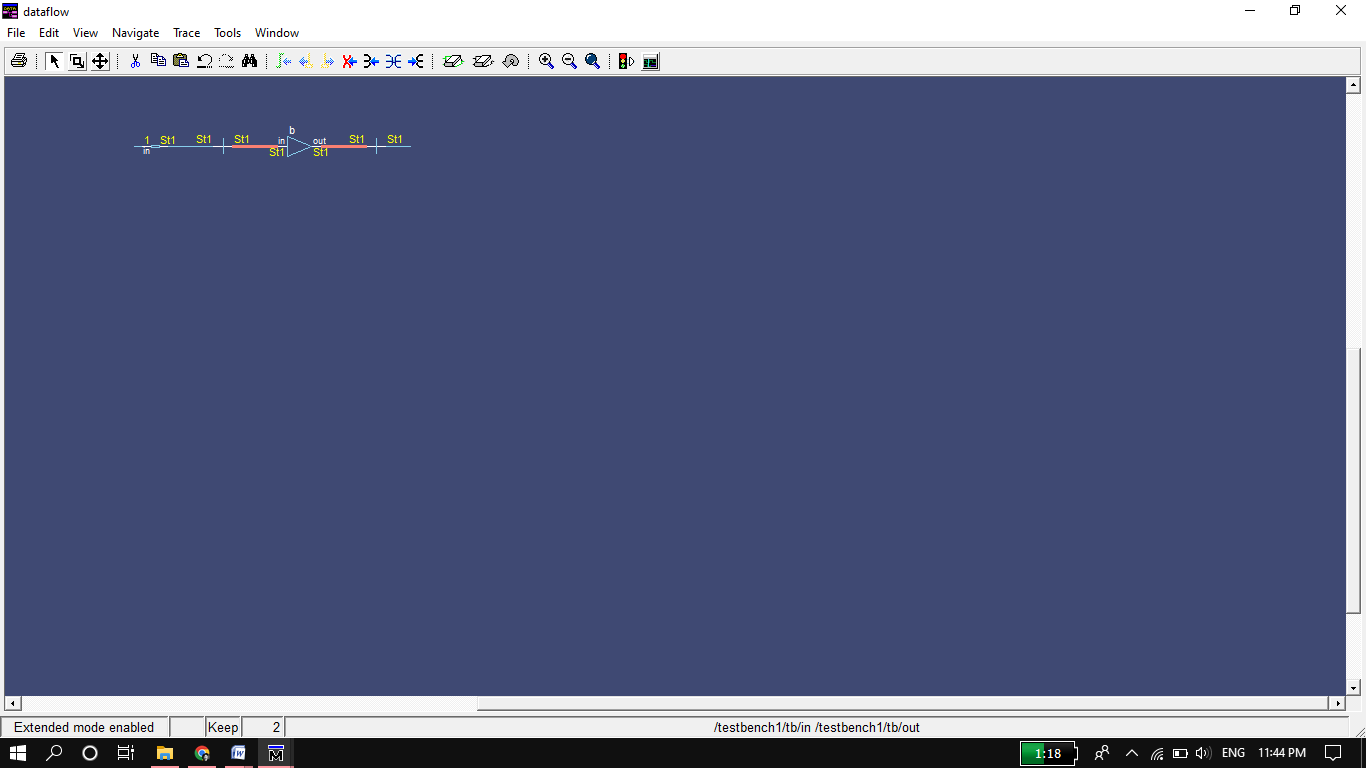
end

endmodule

**Wave output:**



**Circuit:**



**Task 02:** Implement an inverter at the gate level.

**Design code:**

module inverter(in,out);

input in;

output out;

not n(out,in); //output always before input

endmodule

**Test bench:**

module testbench1();

reg in;

wire out;

inverter tb(in,out);

initial

begin

$display("in, Out");

in=0;

#10 $display("%b,%b",in,out);

in=1;

#10 $display("%b,%b",in,out);

in=0;

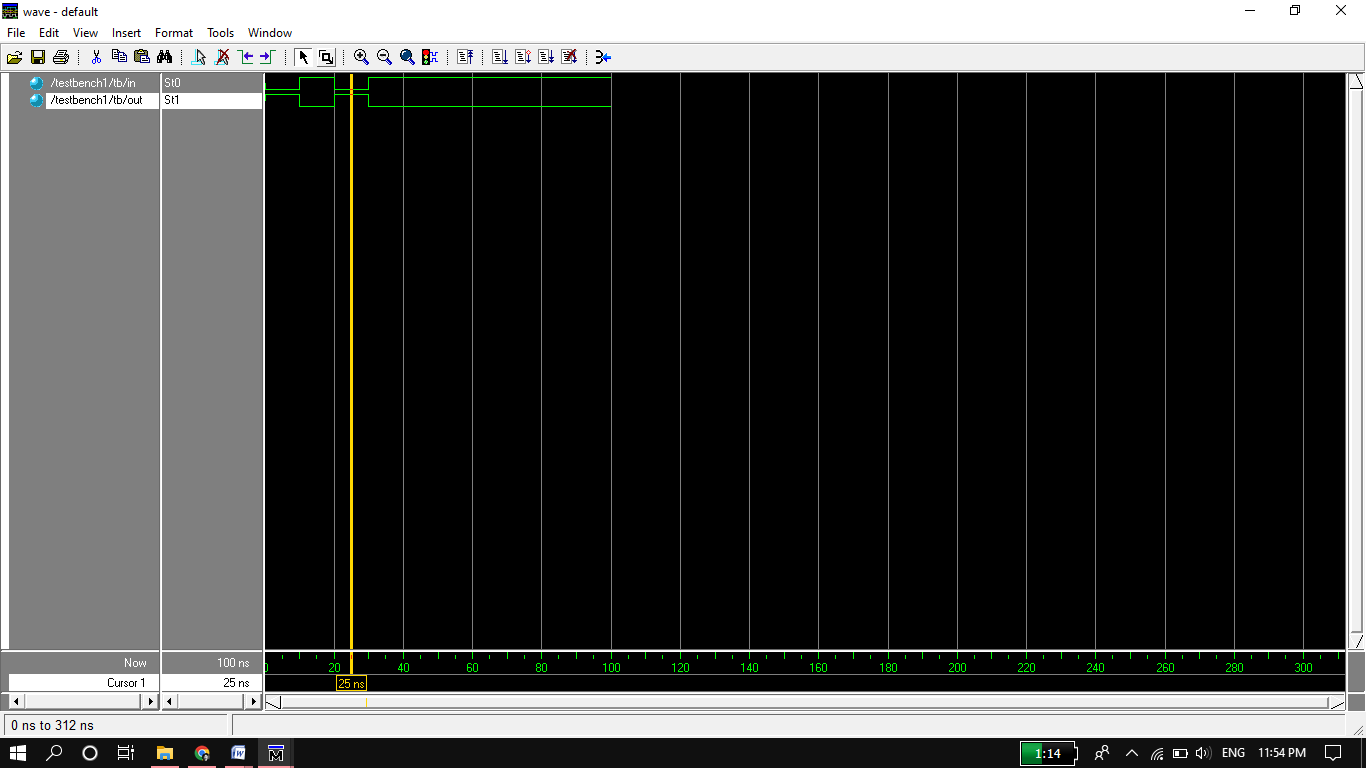
#10 $display("%b,%b",in,out);

in=1;

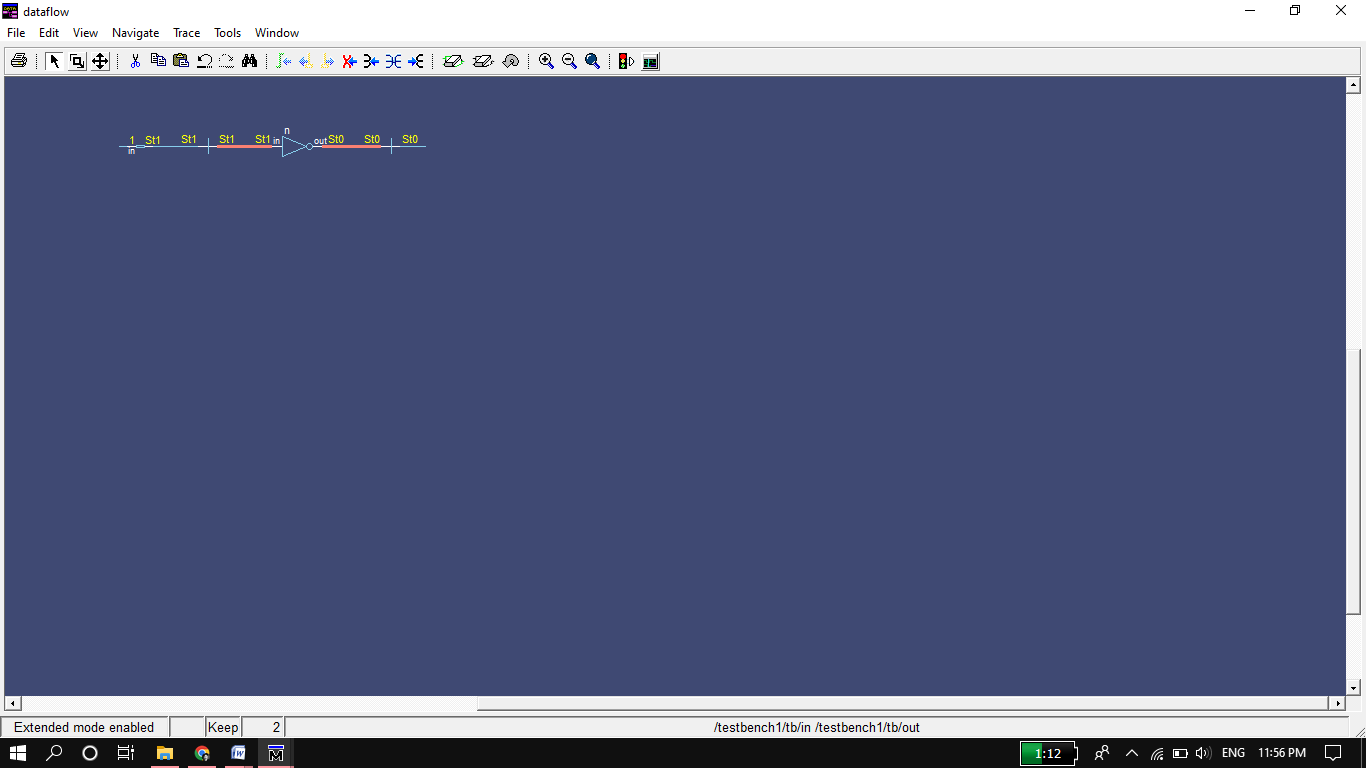
#10 $display("%b,%b",in,out);

end

endmodule

**Wave form:** 

**Circuit:**



**Task 03:** Implement OR gate Using NAND gate.

**Design Code:**

module OR(A,B,C);

input A,B;

output C;

wire w1,w2;

nand n1(w1,A);

nand n2(w2,B);

nand n3(C,w1,w2);

endmodule

**Test Bench:**

module testbench1();

reg A,B;

wire C;

OR tb(A,B,C);

initial

begin

$display("A,B,C");

A=0;B=0;

#20 $display("%b,%b,%b",A,B,C);

A=0;B=1;

#20 $display("%b,%b,%b",A,B,C);

A=1;B=0;

#20 $display("%b,%b,%b",A,B,C);

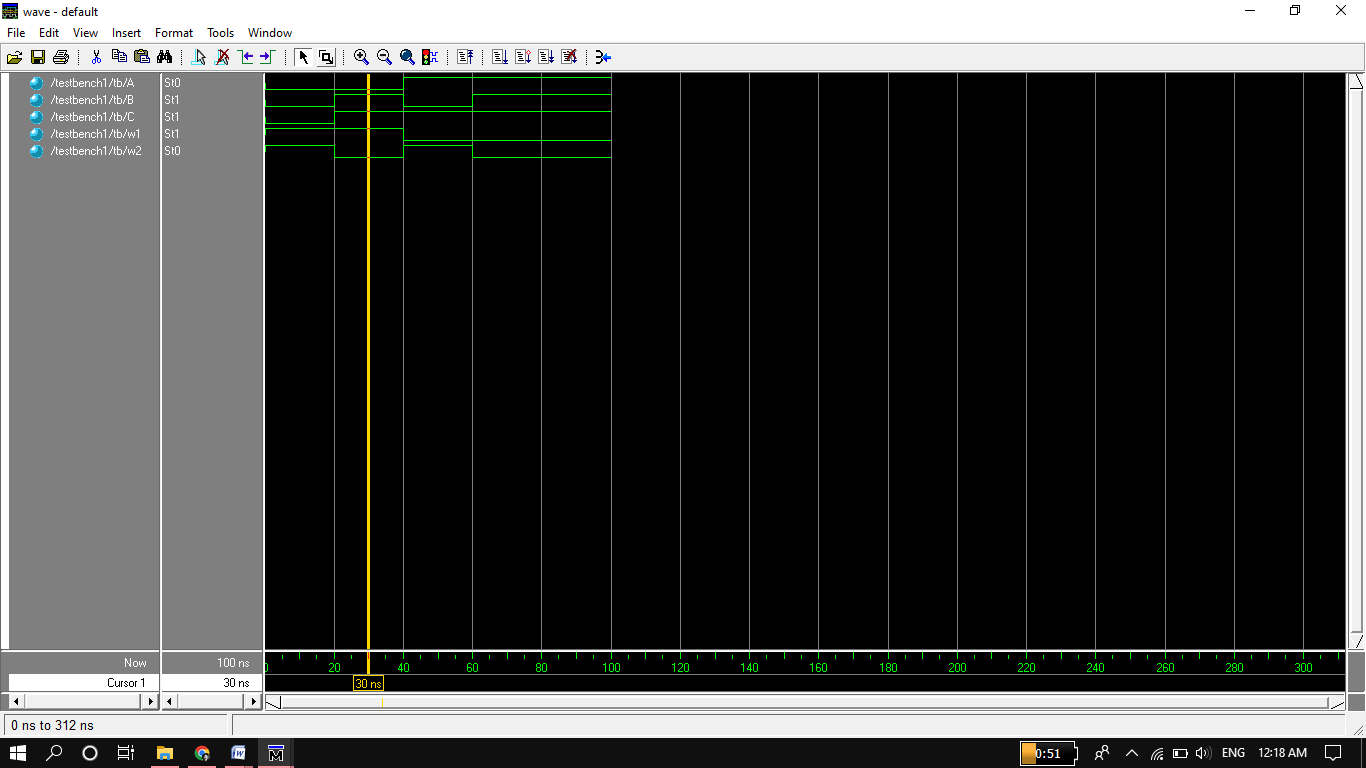
A=1;B=1;

#20 $display("%b,%b,%b",A,B,C);

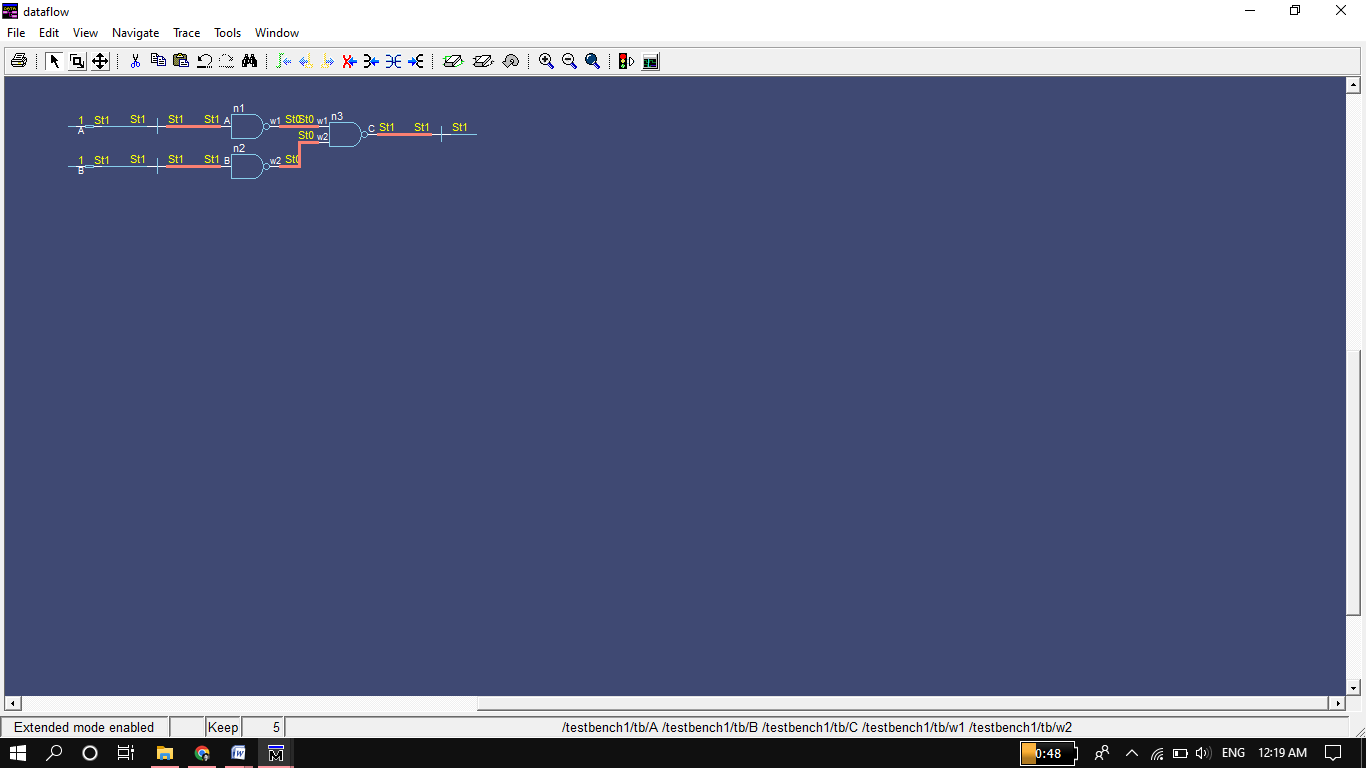
end

endmodule

**Wave Form:**



**Circuit:**



**Task 04:**

Implement the following equation where z is output and x1, x2, x3, x4, and x5 are inputs of the circuit.

z = ( y1 + y2 )’

y1=(x1.x2)

y2 =(x3.x4.x5)

**Design Code:**

module equation(x1,x2,x3,x4,x5,z);

input x1,x2,x3,x4,x5;

output z;

wire y1,y2,nz;

and a1(y1,x1,x2);

and a2(y2,x3,x4,x5);

or o1(nz,y1,y2);

not n1(z,nz);

endmodule

**Test Bench:**

module testbench1();

reg x1,x2,x3,x4,x5;

wire z;

equation tb(x1,x2,x3,x4,x5,z);

initial

begin

$display("x1,x2,x3,x4,x5,z");

x1=0;x2=0;x3=0;x4=0;x5=0;

#20 $display("%b,%b,%b,%b,%b,%b",x1,x2,x3,x4,x5,z);

x1=0;x2=0;x3=0;x4=0;x5=1;

#20 $display("%b,%b,%b,%b,%b,%b",x1,x2,x3,x4,x5,z);

x1=0;x2=0;x3=0;x4=1;x5=0;

#20 $display("%b,%b,%b,%b,%b,%b",x1,x2,x3,x4,x5,z);

x1=0;x2=0;x3=3;x4=0;x5=0;

#20 $display("%b,%b,%b,%b,%b,%b",x1,x2,x3,x4,x5,z);

x1=0;x2=2;x3=0;x4=0;x5=0;

#20 $display("%b,%b,%b,%b,%b,%b",x1,x2,x3,x4,x5,z);

x1=1;x2=0;x3=0;x4=0;x5=0;

#20 $display("%b,%b,%b,%b,%b,%b",x1,x2,x3,x4,x5,z);

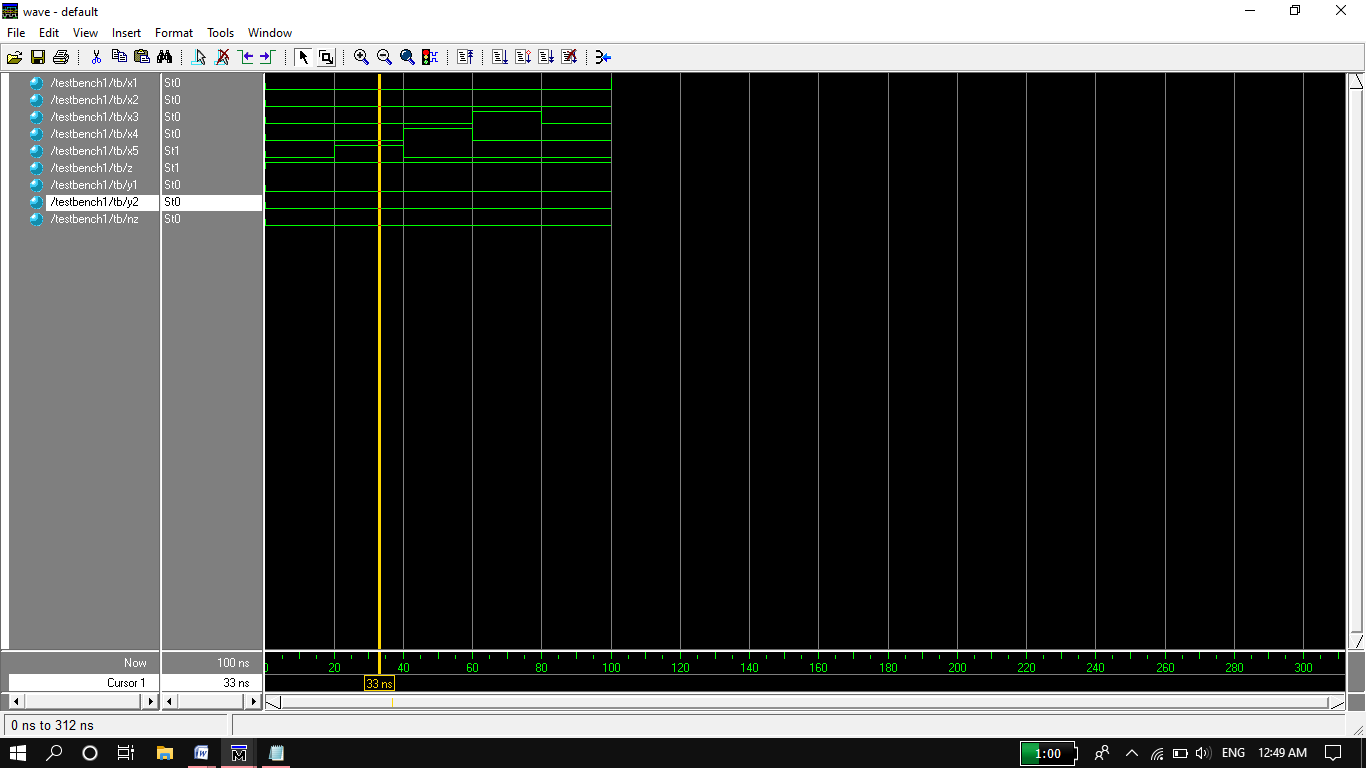
x1=1;x2=1;x3=1;x4=1;x5=1;

#20 $display("%b,%b,%b,%b,%b,%b",x1,x2,x3,x4,x5,z);

end

endmodule

**Wave Form:**



**Circuit:**

